Distributors supplying first all-in-one PC from Raspberry Pi

Farnell and OKdo are supplying the new Raspberry Pi 400, an all-in-one personal computer, created by Raspberry Pi and based on the popular Raspberry Pi 4 single-board computer.

Taking the form of a keyboard, the Raspberry Pi 400 enables users to simply plug in a USB-C based power supply, mouse and micro-SD card configured with a suitable operating system, such as Raspberry Pi OS, to start exploring the world of computing and electronics.

At the heart of Raspberry Pi 400 is the 64-bit BCM2711 system-on-chip, which integrates a quad-core Arm Cortex-A72 CPU running at 1.8GHz, and a VideoCore VI graphics processor supporting OpenGL ES 3.1 and Vulkan graphics, H.264 and H.265 video, and sophisticated image processing capabilities. 4GB of LPDDR4-3200 DRAM provides space for the most demanding use cases.

The Raspberry Pi 400 provides a variety of connectivity and interfacing options: two USB 3.0 ports and a single USB 2.0 port for peripherals; two micro-HDMI ports, supporting up to 4k resolution; Gigabit Ethernet, 802.11ac wireless networking and Bluetooth 5; and a standard 40-pin GPIO port, supporting Raspberry Pi HAT expansion boards.

Raspberry Pi 400 is available on its own, or as part of a kit containing a power supply, a mouse, an HDMI lead, a 16GB micro-SD card with Raspberry Pi OS preinstalled, and a copy of the Raspberry Pi Beginner's Guide.

HoriZone RA development kit

NEW DEVELOPMENT KIT TARGETS EDGE-TO-CLOUD IOT APPLICATIONS. **NEIL TYLER** REPORTS

Avnet Silica has launched the HoriZone RA development kit, which is designed to enable 'proof-of-concept' for edge-to-cloud Internet of Things (IoT) applications requiring secure communications.

Powered by Renesas Advanced (RA) microcontrollers for secure IoT endpoints and edge devices, the kit delivers enhanced security features for Resource Constrained Embedded Systems (RCES) connected to Avnet´s IoTConnect Cloud Platform based on the Microsoft Azure cloud.

The multi-sensor solution is highly scalable, providing a seamless path from proof-of-concept to project through to deployment, including all the required building blocks. The kit includes sensors for humidity, temperatures, ambient light, air quality and air pressure, plus microphone, digital accelerometer, digital gyroscope, and inductive proximity sensor for positioning information.

The board integrates several components from Renesas, including the RA RA6M3 microcontroller, which is suitable for IoT applications that require TFT, Ethernet, security, large embedded RAM, and USB High Speed (HS). Also included are the ISL88014 voltage supervisor and ISL80102 synchronous boost converter for power management. Out of the box, engineers will be able to quickly start developing IoT endpoint and edge devices for a broad range of applications, including industrial and building automation, metering, healthcare, and home appliances.

"IoT growth has increased embedded design complexity exponentially," said Juerg Siegenthaler, Manager 3rd Party Management Avnet Silica. "IoT devices are complex, and with shortening project timelines, the HoriZone cloud-ready platform has all the necessary building blocks that offers designers a ready-made and highly scalable solution for developing new IoT use cases quickly."

HES-DVM simulation flow for FPGA designs

Aldec, an expert in mixed-HDL language simulation and hardware-assisted verification for ASIC and FPGA designs, has introduced a HES-DVM simulation acceleration flow for Microchip's PolarFire, SmartFusion2 and RTSX/RTAX FPGA designs using its HES-MPF500-M2S150 prototyping board

Simulation acceleration techniques have been around for some time, but most products are based on FPGAs from one or two leading FPGA vendors. Usually, it does not matter which FPGA family is used on the simulation acceleration board if the design is coded using synthesizable RTL.

However, growing design complexity, along with shrinking design cycles and shorter time to market, are taking engineers down the path of re-usable IP blocks from the FPGA vendor, instead of developing RTL code. The drawback with this is that the designs become dependent on the given FPGA technology, and the re-usable IP blocks usually require far more computational power to simulate than pure RTL code.

Aldec's HES-DVM looks to overcome these challenges and removes a key verification bottleneck. With the latest release of this powerful EDA tool, users of PolarFire, RTAX/RTSX and SmartFusion2 devices wishing to take advantage of Microchip IPs can accelerate their RTL simulations using Aldec's HES-MPF500-M2S150, which features the largest devices available in both families.