Evaluation of High Performance Compute Architectures

Thorsten Wilmer, Visteon ADAS System Architect

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Agenda

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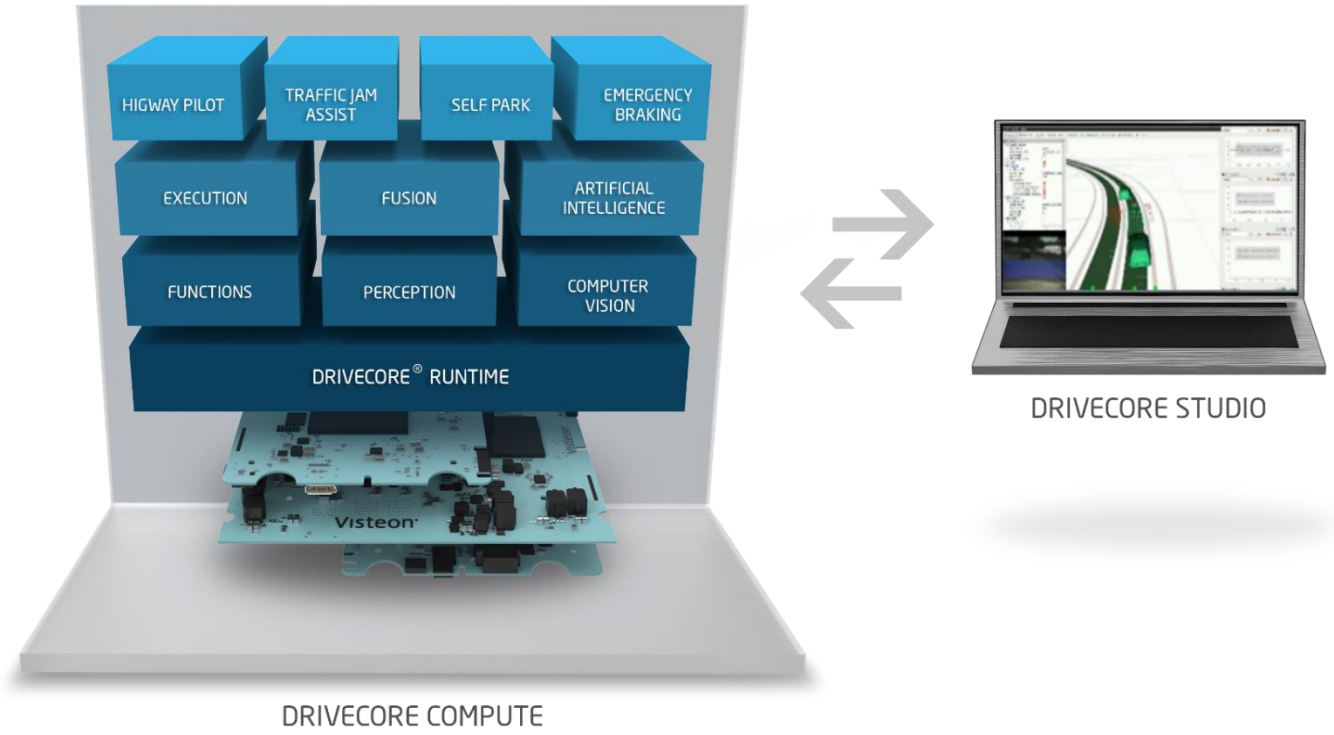
- Overview
- Comparisons
  - Costs
  - Performance Benmarking
  - Communication Latencies
- Conclusion

DriveCore™

Visteon's Autonomous Driving Platform

- DriveCore™ Studio: OPEN for Common Development
- DriveCore™ Compute: Modular Design with SoC Flexibility
- DriveCore™ Runtime: Safe Communication and Easy Integration in Vehicle



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Compute | Runtime | Studio

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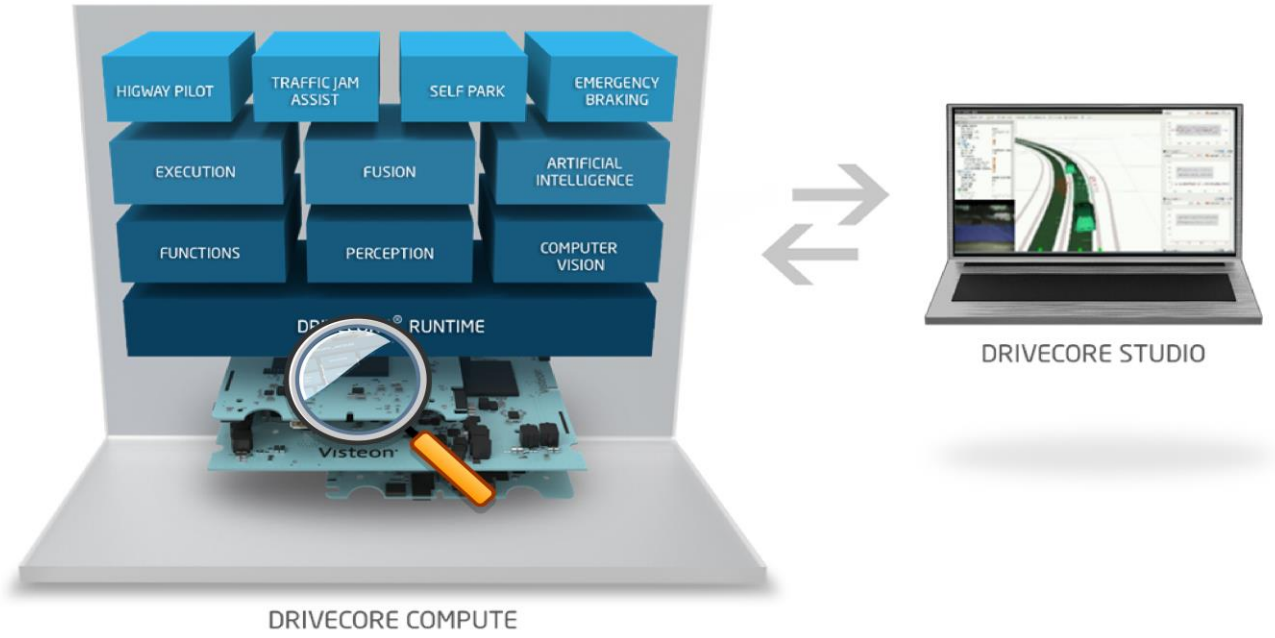

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Compute | Runtime | Studio

Performance Optimization

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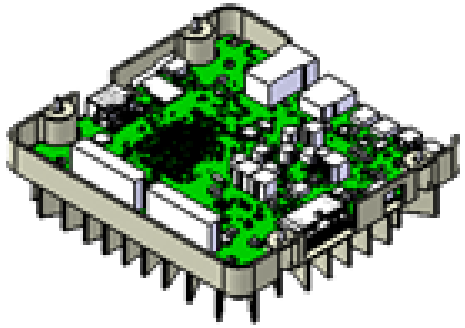
Costs

Computational Performance



Safety

Memory Bandwidth

Communication Performance

Due to NDAs no DriveCore HW was used for public Evaluation

Performance Optimization

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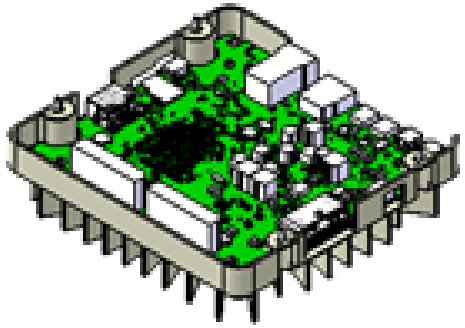


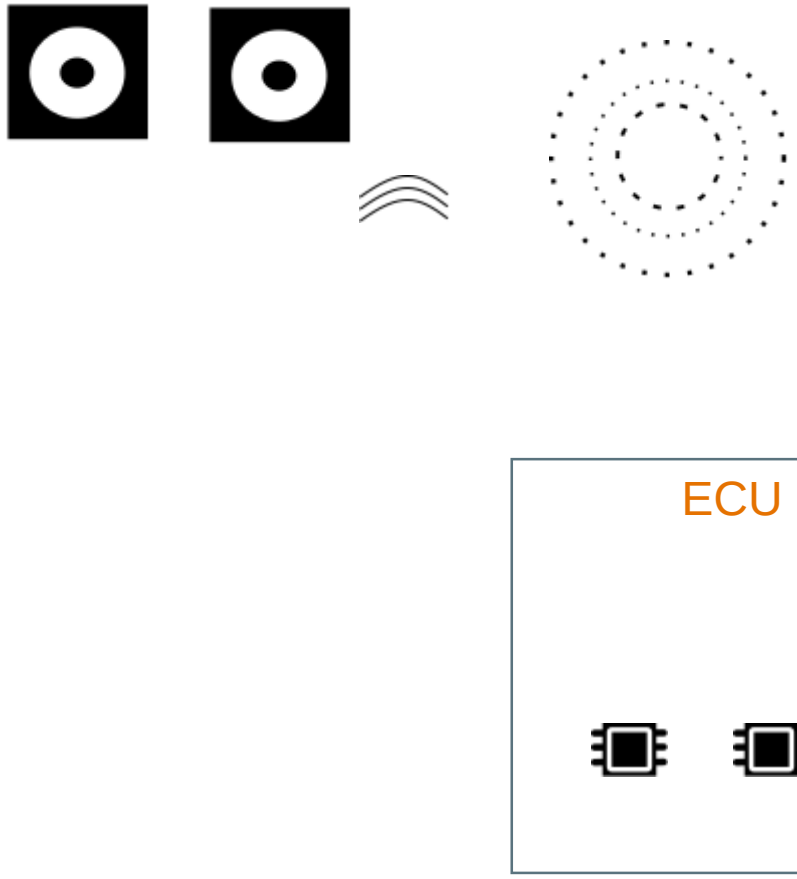
Safety

Memory Bandwidth

Communication Performance

Redundancies On All Levels

- Two front cameras
- Lidar, radar and camera
- Redundant ECUs
- Redundant SoCs
- Redundant virtual partitions
- Redundant SWC
- ECC and repetition of messages
- Repetition of the execution
- Plausibility checks
- HW ECC on busses
- HW lock step
- Tipple voting gates



Resilient System Design

Functional Safety

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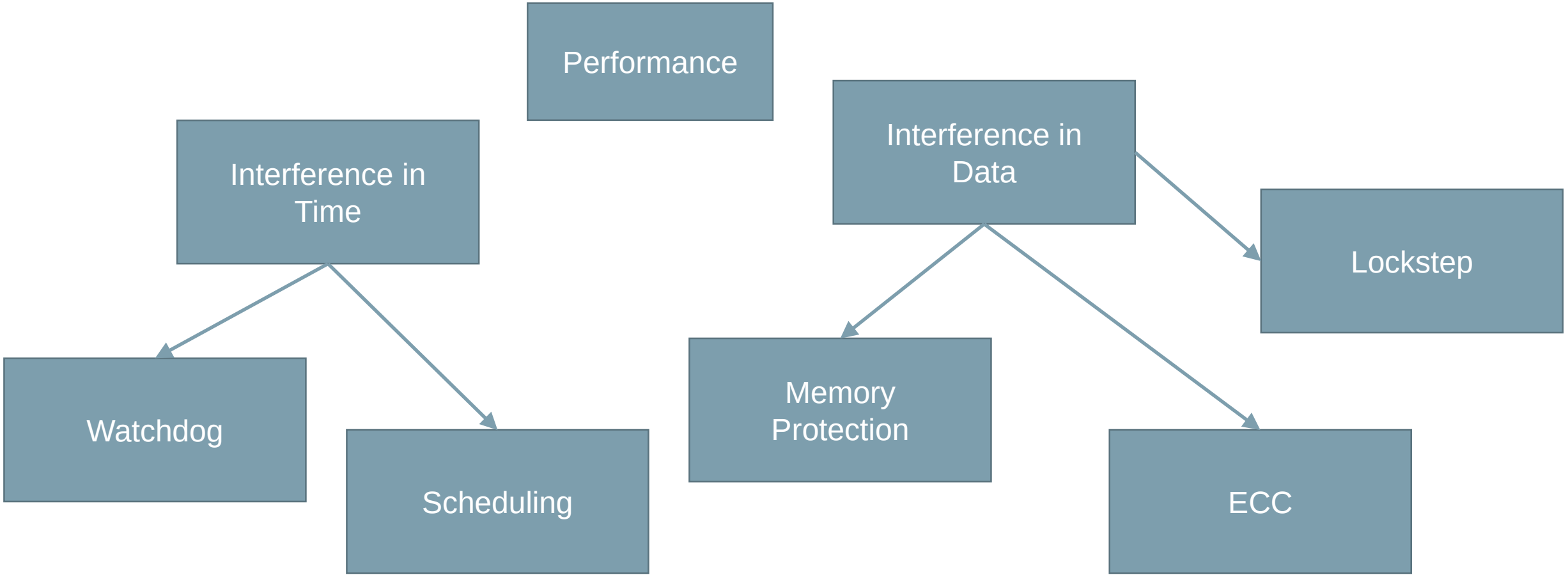


Software and Hardware

Software and Hardware

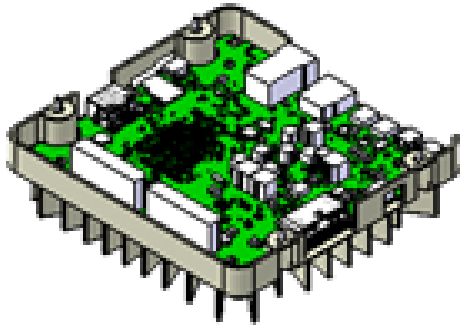
Not every SoC supports all Safety features

Performance Optimization

Visteon

Costs

Safety



Computational Performance

Memory Bandwidth

Communication Performance

Costs

- Scalable SoC
- Scalable System
- Unused features cost
- Searching cheapest Solution which solves the Problem

Choice to select different SoC

Performance Optimization

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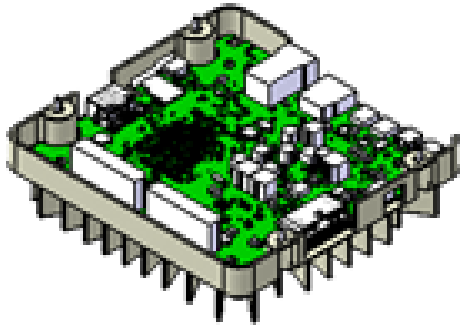
Costs

Safety

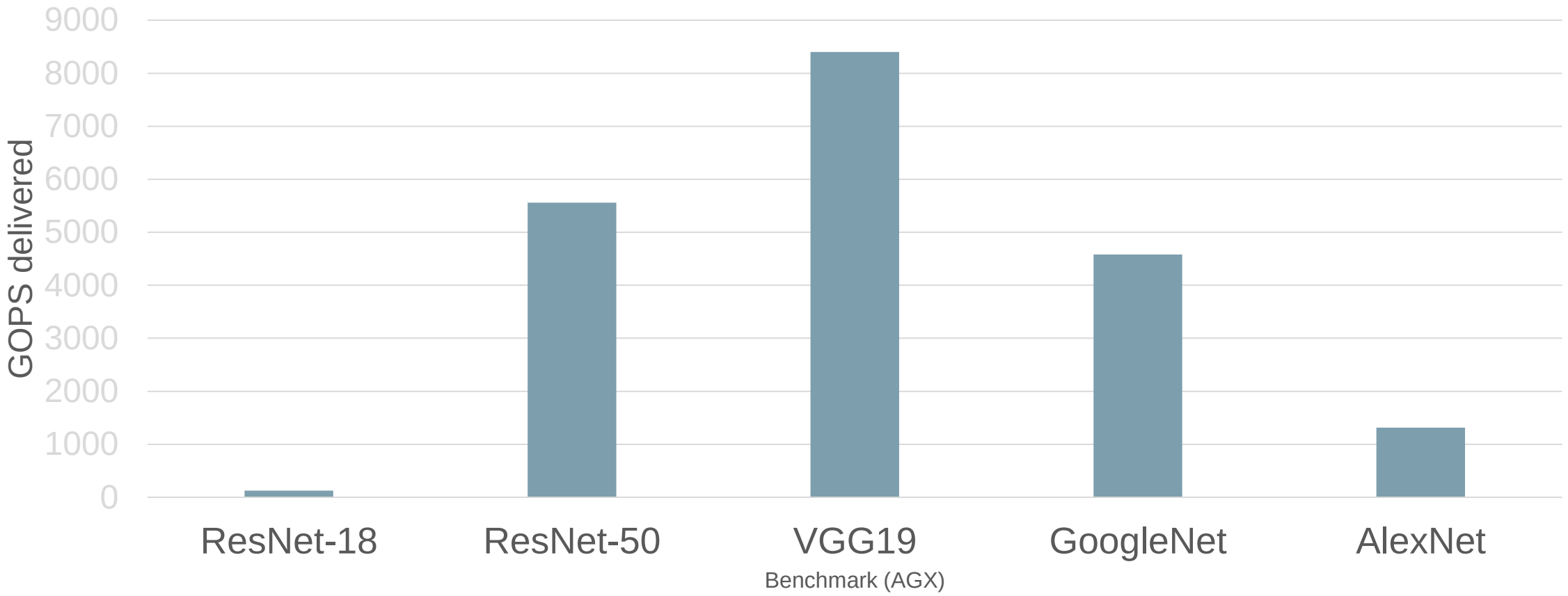


Computational Performance

Memory Bandwidth

Communication Performance

Benchmarking



Source:
https://developer.nvidia.com/embedded/jetson-agx-xavier-dl-inference-benchmarks
https://github.com/albanie/convnet-burden

Different Benchmarks deliver different performance

Computational Performance

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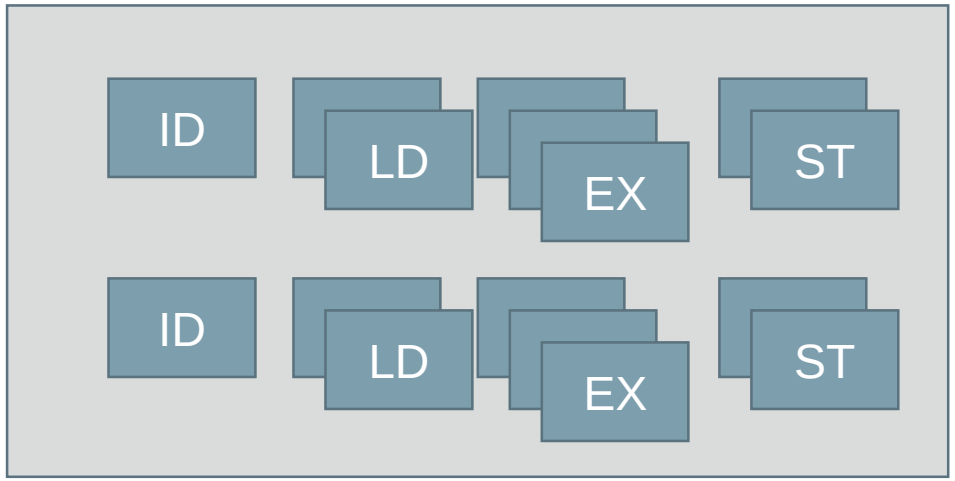
- Operations per Clock
- Pipeline Depth, penalty of Branches
- Register Set Size
- Parallelizm
  - Pipelining
  - Parallel Step Execution
  - Multi Threading
  - Multi Cores



Computational Performance

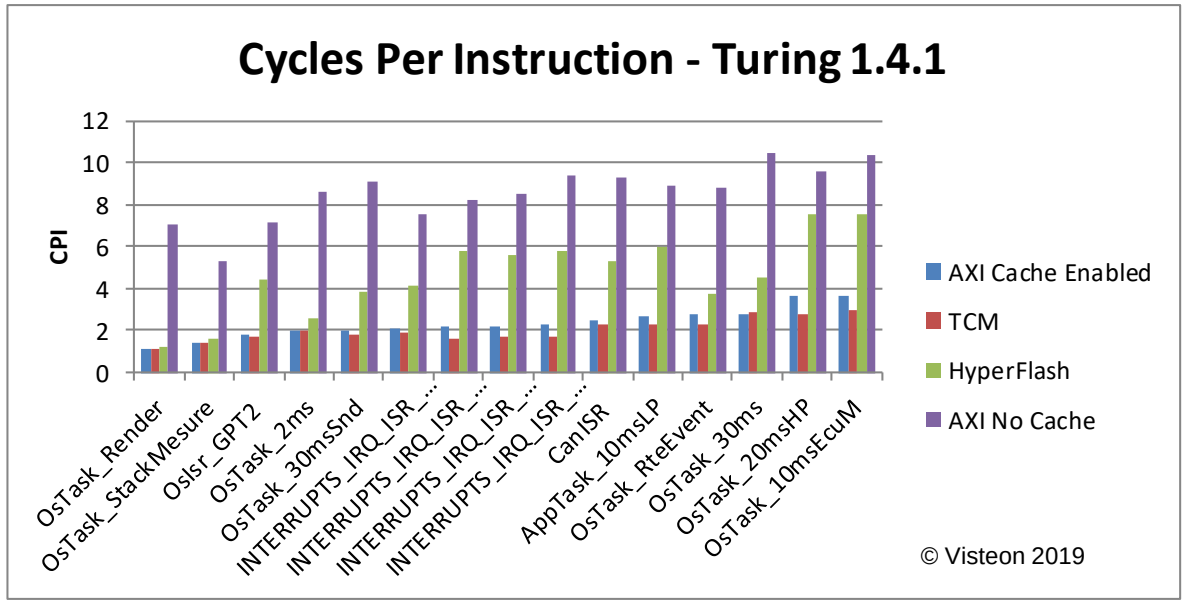
Visteon

Reality

- Not utilized Instruction slots
- Not enough parallelizm
- Cache misses (size, associativity)
- Memory Bandwidth limitation
- Branch Miss prediction
- Random Access Patterns
- Inefficient imlementaion

Theroy

- Clock Cycle each Execution unit is performing one usefull Operation



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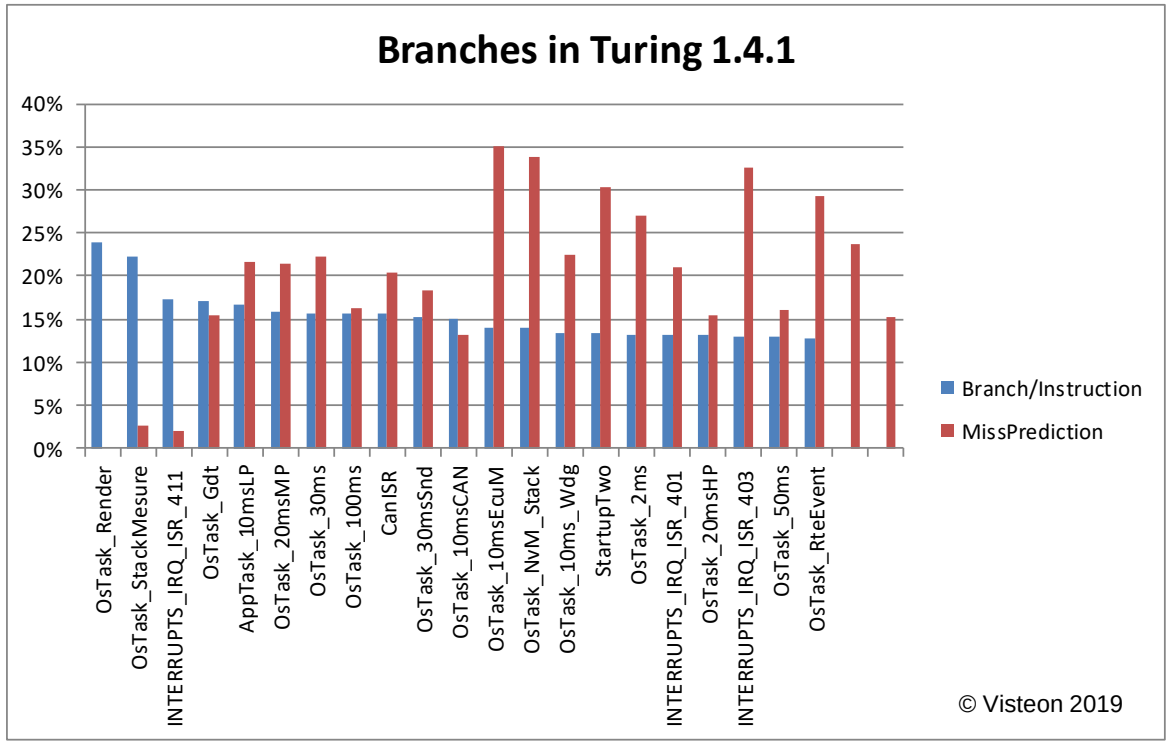
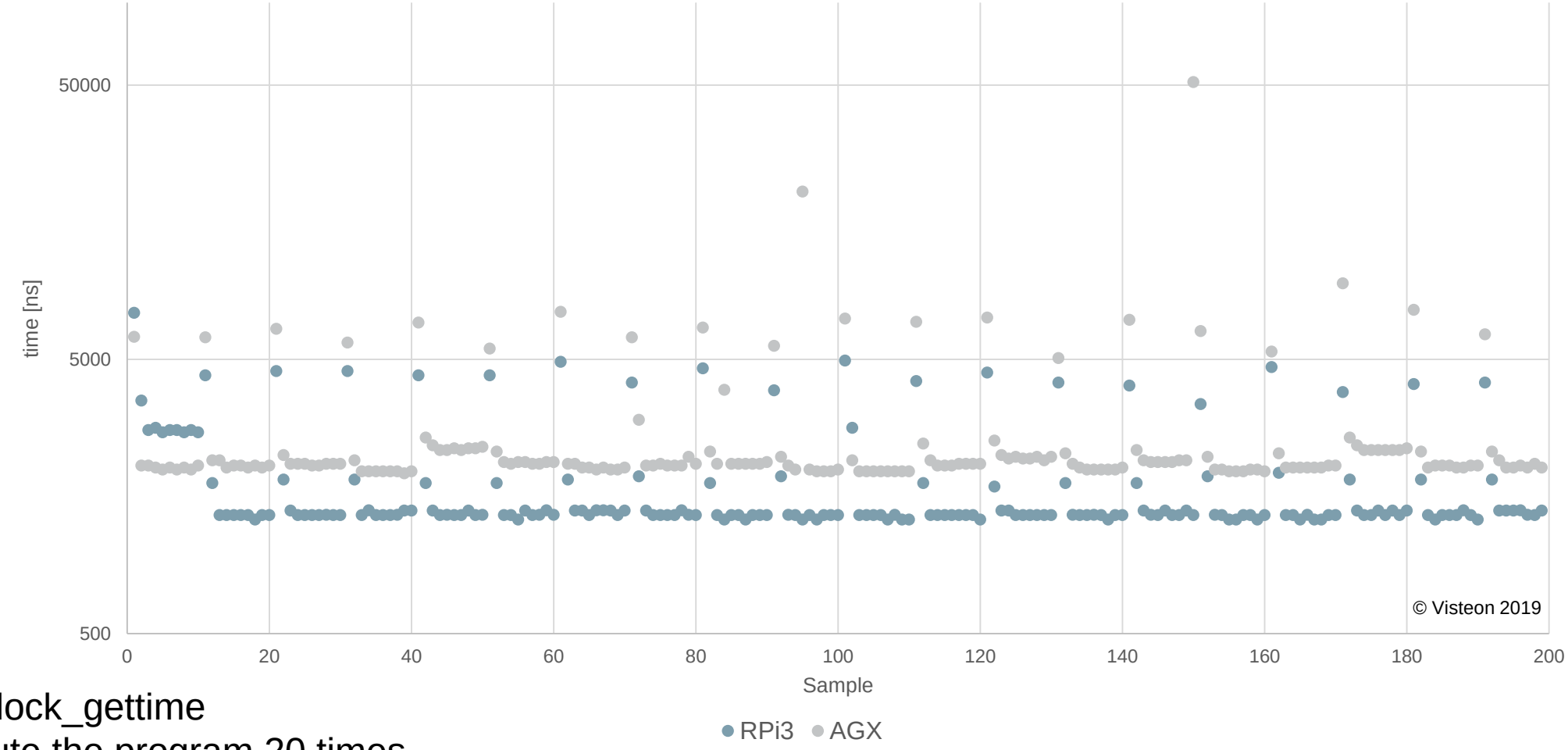


Measurement overhead



- 10x clock_gettime
- Execute the program 20 times

Cache effects

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Use performance counters to measure

Performance Optimization

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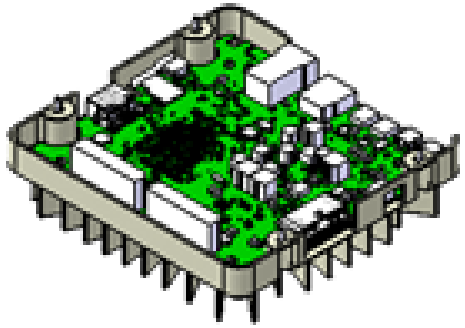
Costs

Safety

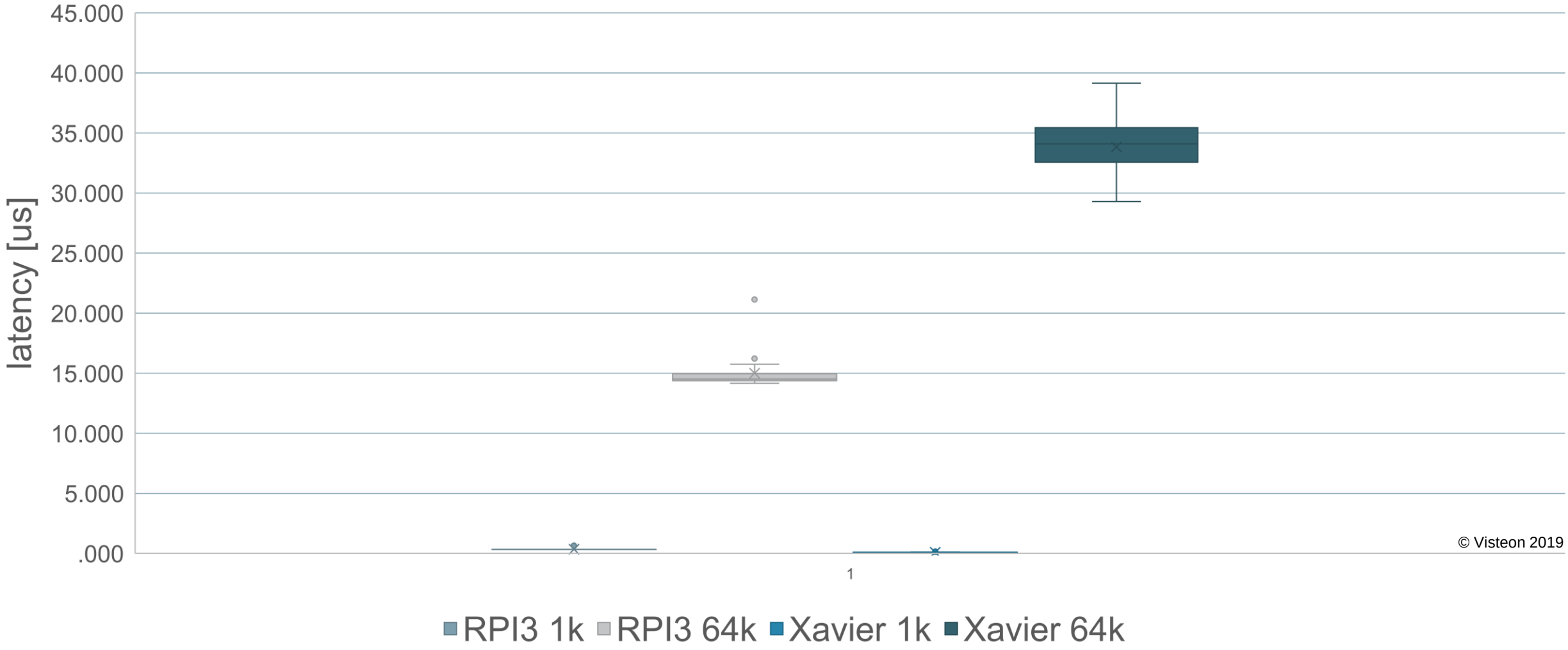


Computational Performance

Memory Bandwidth

Communication Performance

Memory Latency of Messages



Latency depends on the size of a message

Performance Optimization

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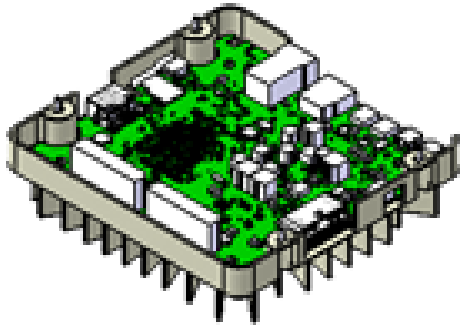
Costs

Safety



Computational Performance

Memory Bandwidth

Communication Performance

Measure UDP Round Trip Time

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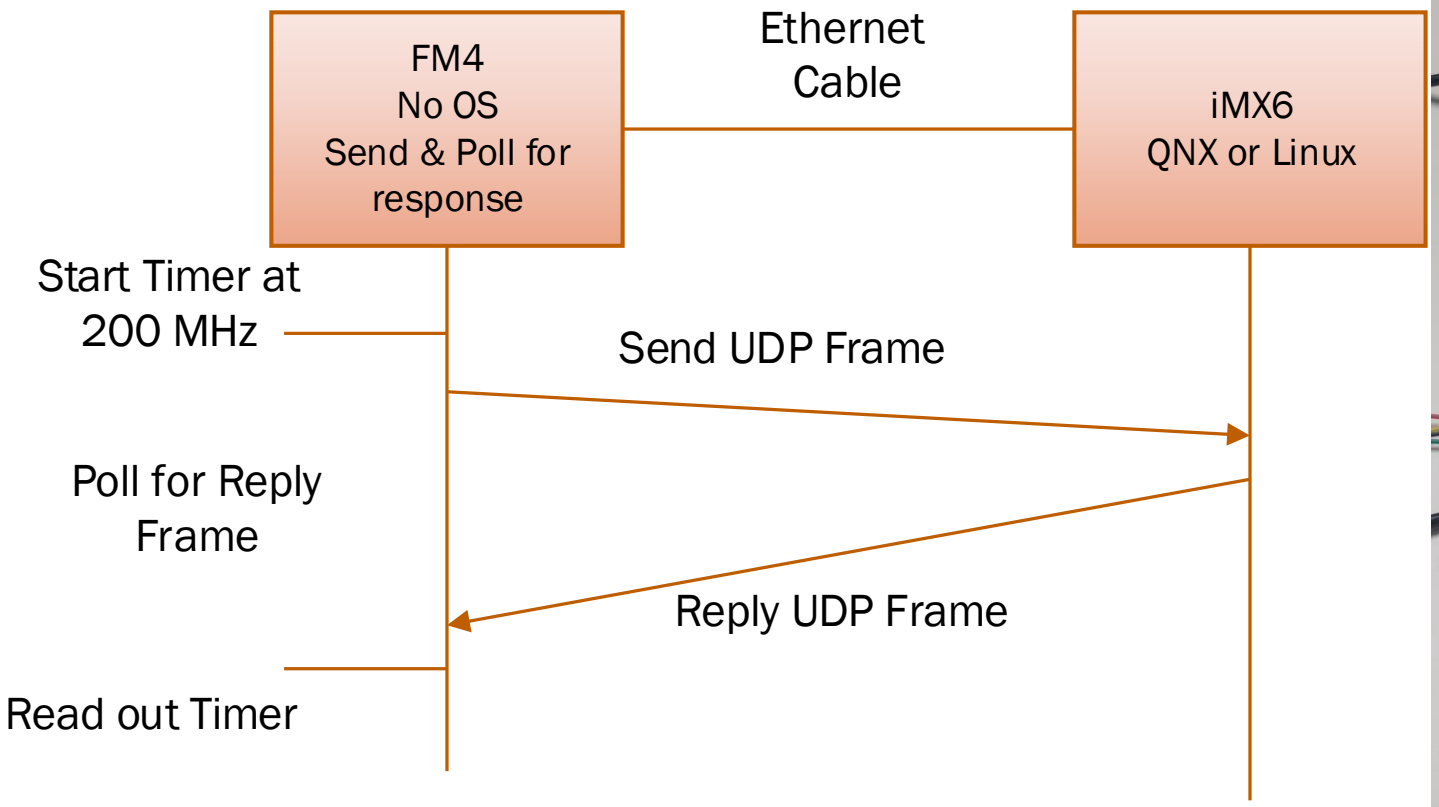
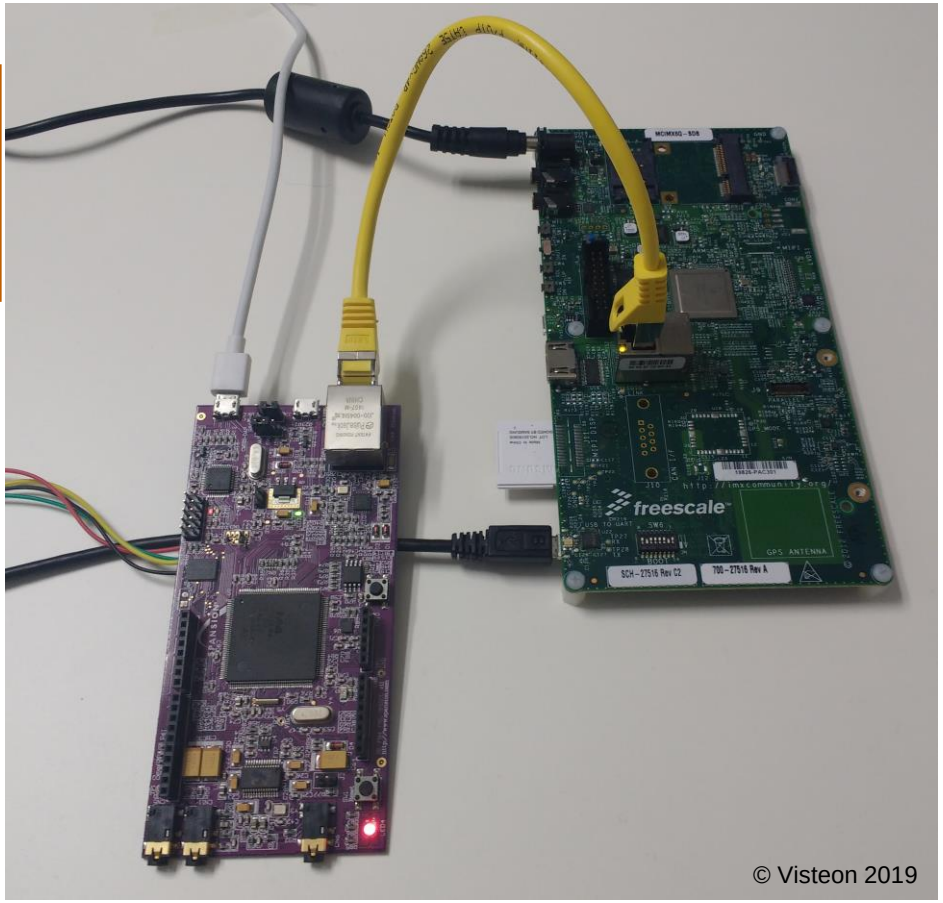
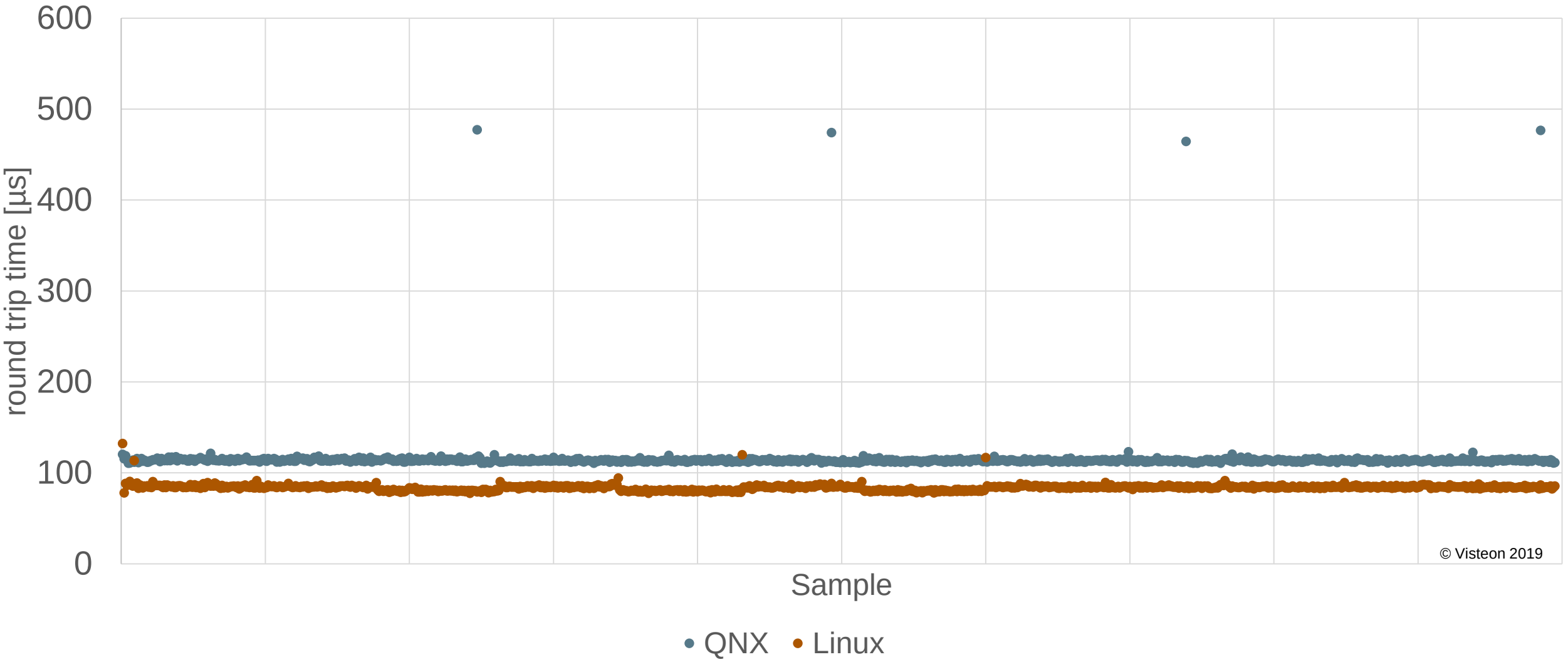




Prefer bare metal HW to measure timings

Link: https://github.com/a01b2080

UDP Round Trip Time



Without optimization Linux has better UDP Latency

Conclusion

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- It is not possible to find “the” best SoC
- Key is how Software uses Hardware
- Latency is a concern

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